forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material.

51. (Amended) The process as recited in claim 50, wherein an overall depth of said trench is two times the depth of a bordering diffusion region.

REMARKS

Favorable consideration of the application is respectfully requested. Claims 25-31, 33-38, 40-41, 43-44, 50-54 and 56, prior to this paper were pending in the present application. By this paper, claim 44 is canceled, without prejudice, and claims 25, 26, 34, 35, 40, 41, 50 and 51, are amended.

Election/Restrictions

The Examiner determined that previously elected claim 44 reads on non-elected Species II. Therefore, claim 44 has been canceled, without prejudice.

Claim Rejections - 35 U.S.C. §112

Claim 25, prior to amendment, was rejected for insufficient antecedent basis.

The word "semiconductive" has been removed in claim 25.

Claims 26, 35, 41 and 51, prior to amendment, were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 26, 35, 41 and 51 have been amended by deleting the phrase "where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms."

Thus, by amendment, the rejection of claims 25, 26, 35, 41 and 51under 35 U.S.C. §112, second paragraph, is overcome.

Claim Rejections - 35 U.S.C. §102

Claims 50-54 and 56, prior to amendment, were rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki (U.S. Patent 4,471,525).

Base claim 50 has been amended to recite:

> "...forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material,"

language which further distinguishes the presently claimed invention from Sasaki.

Sasaki does not teach or suggest forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material, a feature of the presently claimed invention as relied for amendment.

Thus, claim 50, as presently amended, is patentable over the art of record and thus place dependent claims 51-54 and 56 as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 50-54 and 56, under 35 U.S.C. §102(b), as being anticipated by Sasaki, is overcome.

Claims 25-29, 33, 50, 52 and 56, prior to amendment, were rejected under 35 U.S.C. §102(e) as being anticipated by Akram (U.S. Patent 5,895,253).

Base claims 25 and 50 have been amended to recite:

> "...forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material,"

language which further distinguishes the presently claimed invention from Akram.

Akram does not teach or suggest forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material, a feature of the presently claimed invention as relied for amendment.

Thus claims 25 and 50, as presently amended, are patentable over the art of record and thus place the remaining respective dependent claims 26-29, 33, 52 and 56 as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 25-29, 33, 50, 52 and 56, under 35 U.S.C. §102(e), as being anticipated by Akram, is overcome.

Claim Rejections - 35 U.S.C. §103

Claims 25-31, 33-38, 40-41 and 43, prior to amendment, were rejected under 35 U.S.C. §103(a) as being unpatentable over Sasaki in view of Kameyama (U.S. Patent 4,472,240).

Base claims 25, 34 and 40 have been amended to recite:

> "...forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material,"

language which further distinguishes the presently claimed invention from Sasaki in view of Kameyama.

Sasaki in view of Kameyama do not teach or suggest forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material, a feature of the presently claimed invention as relied for amendment.

Thus, base claims 25, 34 and 40, as presently amended, are patentable over the art of record and thus place the remaining respective dependent claims 26-31, 33, 35-38, 41 and 43 as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 25-31, 33-38, 40-41 and 43, under 35 U.S.C. §103(a), as being unpatentable over Sasaki in view of Kameyama, is overcome.

Additional Information

Attached hereto (**Appendix A**) is a marked-up version of the changes made to the claims per Applicant's present response (paper 7).

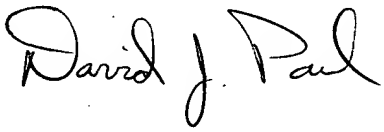
Also, attached hereto (**Appendix B**) is a clean copy of the current pending 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response (paper 7).

CONCLUSION

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,



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APPENDIX A

Following is a marked-up version of the changes made per Applicant's present response in paper 7.

In the Claims:

Claims 25, 26, 34, 35, 40, 41, 50 and 51 have been amended as indicated below.

25. (Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;
forming a spacer along the sidewall of said first trench;
forming a second trench into said [semiconductor] substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;
forming an insulative material in said first and second trenches[, said insulative material] at least partially by substantially consuming said spacer and said dielectric lining to substantially fill[ing] said first and second trenches with said insulative material.

26. (Amended) The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region [where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms].

34. (Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench;

forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming an insulative material in said first and second trenches[, said insulative material] at least partially by substantially consuming said semiconductive spacer and [thereby] said dielectric lining during formation to substantially fill[ing] said first and second trenches with said insulative material;

planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

35. (Amended) The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region [where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms].

40. (Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler in said first and second trenches[, said oxide] at least partially by substantially consuming said silicon spacer and [thereby] and said oxide layer to substantially fill[ing] said first and second trenches with said oxide filler;

planarizing said oxide filler.

41. (Amended) The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region [where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms].

50. (Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;
forming a dielectric lining on the surface of said trench;
forming a semiconductive spacer along the sidewall of said trench;
forming an insulative material in said trench[, said insulative material] at least partially by substantially consuming said semiconductive spacer and [thereby] and said dielectric lining to substantially fill[ing] said trench with said insulative material.

51. (Amended) The process as recited in claim 50, wherein an overall depth of said trench is two times the depth of a bordering diffusion region [where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms].

APPENDIX B

Following is a copy of the current pending claims 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response in paper 7.

25. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;
forming a spacer along the sidewall of said first trench;
forming a second trench into said substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;
forming an insulative material in said first and second trenches at least partially by substantially consuming said spacer and said dielectric lining to substantially fill said first and second trenches with said insulative material.

26. The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

27. The process as recited in claim 25, wherein said spacer is formed from an oxidizable material.

28. The process as recited in claim 25, wherein said spacer is formed of oxide.

29. The process as recited in claim 25, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

30. The process as recited in claim 25, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same material.

33. The process as recited in claim 25, wherein said process uses only one mask to form said device isolation.

34. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;
forming a semiconductive spacer along the sidewall of said first trench;
forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;
forming an insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said dielectric lining during formation to substantially fill said first and second trenches with said insulative material;
planarizing said insulative material;
wherein said process uses only one mask to form said device isolation.

35. The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

APPENDIX B

36. The process as recited in claim 34, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

37. The process as recited in claim 34, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. The process as recited in claim 34, wherein said insulative material and said dielectric lining are the same material.

40. A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;
forming a first trench into said silicon substrate assembly using said mask as an etching guide;
forming an oxide layer on the surface of said first trench;
forming a silicon spacer on the sidewall of said first trench;
forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;
forming an oxide filler in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;
planarizing said oxide filler.

41. The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

43. The process as recited in claim 40, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

50. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;
forming a dielectric lining on the surface of said trench;
forming a semiconductive spacer along the sidewall of said trench;
forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said dielectric lining to substantially fill said trench with said insulative material.

51. The process as recited in claim 50, wherein an overall depth of said trench is two times the depth of a bordering diffusion region.

52. The process as recited in claim 50, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a trench.

53. The process as recited in claim 50, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. The process as recited in claim 50, wherein said insulative material and said dielectric lining are the same material.

56. The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.